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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,105	02/27/2002	Andrew Phelps	5181-97700	6781

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EXAMINER	
CHU, GABRIEL L	

ART UNIT	PAPER NUMBER
2114	5

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,105	PHELPS, ANDREW	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,16 and 31-33* is/are rejected.

7)☒ Claim(s) *2-15 and 17-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 25 is objected to because of the following informalities: Claim 25 is understood to depend from claim 24 instead of claim 23. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 16, and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6308297 to Harris. Referring to claim 1, Harris discloses a memory subsystem comprising: a memory controller configured to generate a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information (From line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22." Further, from the abstract, "In use, an address port receives an address identifying at least one memory location and associated verification information (e.g., parity or error correcting information) for verifying the address."); and a memory module including a plurality of memory chips for storing data (From line 44 of column 2, "In a preferred

implementation, the memory device is an integrated memory chip." Further, from line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22."), wherein said memory module is coupled to receive said plurality of memory requests (From the title, "Method and apparatus for verifying memory addresses".); wherein said memory module further includes an error detection circuit configured to detect an error in said address information based on said corresponding error detection information and to provide an error indication in response to detecting said error (From line 20 of column 2, "Preferably, the verification logic is operable to indicate an error where address verification is negative. More preferably, the memory device comprises an error output for returning an error signal where address verification is negative. The error signal can be used simply to report a fault. Alternatively, it can be used to cause a memory controller to retry a memory addressing operation.").

4. Referring to claim 16, Harris discloses a computer system comprising: a processor (Figure 1, element 12.); a memory subsystem coupled to said processor, said memory subsystem including: a memory controller configured to generate a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information (From line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22." Further, from the abstract, "In use, an address port receives an address identifying at least one memory location and associated verification information (e.g., parity or error correcting information) for verifying the address."); and a memory

module including a plurality of memory chips for storing data data (From line 44 of column 2, "In a preferred implementation, the memory device is an integrated memory chip." Further, from line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22."), wherein said memory module is coupled to receive said plurality of memory requests (From the title, "Method and apparatus for verifying memory addresses".); wherein said memory module further includes an error detection circuit configured to detect an error in said address information based on said corresponding error detection information and to provide an error indication in response to detecting said error (From line 20 of column 2, "Preferably, the verification logic is operable to indicate an error where address verification is negative. More preferably, the memory device comprises an error output for returning an error signal where address verification is negative. The error signal can be used simply to report a fault. Alternatively, it can be used to cause a memory controller to retry a memory addressing operation.").

5. Referring to claim 31 and 32, Harris discloses generating a plurality of memory requests each including address information and corresponding error detection information dependent upon said address information (From line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22." Further, from the abstract, "In use, an address port receives an address identifying at least one memory location and associated verification information (e.g., parity or error correcting information) for verifying the address."); and a memory module receiving each of said plurality of memory requests (From the title, "Method and

apparatus for verifying memory addresses".); said memory module detecting an error in said address information based on said corresponding error detection information; and said memory module providing an error indication in response to detecting said error (From line 20 of column 2, "Preferably, the verification logic is operable to indicate an error where address verification is negative. More preferably, the memory device comprises an error output for returning an error signal where address verification is negative. The error signal can be used simply to report a fault. Alternatively, it can be used to cause a memory controller to retry a memory addressing operation.").

6. Referring to claim 33, Harris discloses a memory subsystem comprising: a memory controller configured to generate a plurality of memory requests each including control information and corresponding error detection information dependent upon said control information (From line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22." Further, from the abstract, "In use, an address port receives an address identifying at least one memory location and associated verification information (e.g., parity or error correcting information) for verifying the address."); and a memory module including a plurality of memory chips for storing data (From line 44 of column 2, "In a preferred implementation, the memory device is an integrated memory chip." Further, from line 55 of column 3, "The address bus 25 is for passing addresses from the memory controller to individual memory devices 22."), wherein said memory module is coupled to receive said plurality of memory requests (From the title, "Method and apparatus for verifying memory addresses".); wherein said memory module further includes an error detection

circuit configured to detect an error in said control information based on said corresponding error detection information and to provide an error indication in response to detecting said error (From line 20 of column 2, "Preferably, the verification logic is operable to indicate an error where address verification is negative. More preferably, the memory device comprises an error output for returning an error signal where address verification is negative. The error signal can be used simply to report a fault. Alternatively, it can be used to cause a memory controller to retry a memory addressing operation.").

Allowable Subject Matter

7. Claims 2-15 and 17-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Referring to claims 2-15 and 17-30, the prior art does not teach or fairly suggest each of said plurality of memory requests further include control information and said corresponding error detection information is further dependent upon said control information, in the scope and context of claims 1 and 16.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 3599146 to Weisbecker

US 4044337 to Hicks et al.

US 5453999 to Michaelson et al.

US 5509119 to La Fetra

US 5944838 to Jantz

US 6742159 to Sakurai

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298, and after approximately October 15, 2004 will be (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

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